CLAIMS

1. A print engine/controller chip configurable to be coupled with others to drive a multi-segment printhead comprising:

a memory buffer for receiving compressed page data;

image decoders to perform an expansion, in pipeline fashion, of the compressed page data;

a half-toner/compositer to composite respective strips of the decoded image planes; and

a printhead interface to output the composite strip to a printhead, the printhead interface including:

a multi-segment printhead interface outputting printhead formatted data; and

a synchronization signal generator outputting a synchronization signal to couple print engine/controllers to synchronize their respective strips at the printhead; and

a micro-controller CPU core.

2. The print engine/controller of claim 1 wherein:

the CPU core performs a QA chip authentication via a serial interface.

3. The print engine/controller of claim 2 wherein:

QA chip authentication occurs between print pages.

4. The print engine/controller of claim 1 wherein:

the CPU core runs a printer's stepper motor via a parallel interface during a print.

5. The print engine/controller of claim 1 wherein:

the CPU core provides a means of interfacing with external data requests.

6. The print engine/controller of claim 1 wherein:

the CPU core provides a means of interfacing with a printhead low-speed

data request.

7. The print engine/controller of claim 6 wherein:
the low-speed data request is a characterization vector.

8. The print engine/controller of claim 6 wherein:
the low-speed data request is a writing pulse profile.

9. The print engine/controller of claim 1 wherein:
the CPU core does not process pixels.

10. The print engine/controller of claim 1 wherein:
the CPU core is associated with a program ROM and a program scratch RAM.

11. The print engine/controller of claim 1 wherein:
the pipeline fashion expansion is performed using a high speed serial interface, a standard JPEG decoder 28, a standard Group 4 Fax decoder, a half-toner/compositor unit, a tag encoder, a line loader/formatter unit.

12. The print engine/controller of claim 11 wherein:
the decoders and encoder are buffered to the half-toner/compositor.

13. The print engine/controller of claim 12 wherein:
the high speed serial interface is an IEEE 1394 interface.

14. The print engine/controller of claim 1 wherein:
the printhead interface is adapted to receive an input signal that determines if the print engine controller is a master controller or a slave.

15. The print engine/controller of claim 1 wherein;
the halftoner/compositor scales input image planes under control of a margin unit set to establish print data for a strip of the image.

16. The print engine/controller of claim 1 wherein:

the pipeline fashion expansion further comprises the expansion, in parallel, of a JPEG-compressed contone CMYK layer and at least one other layer.

17. The print engine/controller of claim 16 wherein:

the other layer is a Group 4 Fax-compressed bi-level black layer.

18. The print engine/controller of claim 17 wherein:

the pipeline fashion expansion further comprises the expansion, in parallel with the layers, of a Group 4 Fax-compressed bi-level dither matrix selection map.

19. The print engine/controller of claim 18 further comprising:

a tag encoder for encoding bi-level infra-red tag data from the compressed page data.

20. The print engine/controller of claim 19 wherein:

the pipeline fashion expansion further comprises a second stage dithering of the contone CMYK layer using a dither matrix selected by the dither matrix select map.